Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-8. (Cancelled)

9. (Currently Amended) A dual damascene process comprising:

on a first wiring layer, providing a dielectric layer having an upper surface and a thickness;

forming a via hole that extends from said upper surface to said first wiring layer;

patterning and etching said dielectric layer, thereby forming a trench having a bottom surface, a mouth, and side walls, said trench being disposed so as to fully overlap said via hole and to extend a depth below said upper surface, said depth being ~~between about 0.5 and 2 times said dielectric thickness whereby~~ greater than a depth of said via hole, wherein the depth of the via hole extends a distance from said trench bottom surface to the first wiring layer ~~that is between about 0.5 and 2 times said dielectric thickness~~;

by means of PVD, depositing a seed layer of metal to coat the dielectric layer; said bottom surface, and said side walls;

~~sputter etching~~ reducing the seed layer~~, to reduce its thickness~~ by an amount~~, thereby preferentially removing~~ to remove any overhang present at the mouth of the trench;

~~depositing metal to form~~ forming a filler layer that overfills the trench and via hole; and

planarizing said filler layer~~, thereby just filling the trench with metal, forming a second wiring layer, removing any metal that is outside the trench, and forming~~ to form a metal conductive via whose aspect ratio is less than about 6:1 whereby its electrical resistance is less than about ~~0.1 ohms~~ 1 ohm.

10. (Original) The process described in claim 9 wherein the metal is selected from the group consisting of copper, gold, and silver.

11. (Original) The process described in claim 9 wherein the metal is copper and said electrical resistance is less than about 1 ohm.

12. (Currently Amendment) A process for filling an opening, comprising:

providing a power supply having high and low voltage settings;

providing an integrated circuit having an upper surface;

removing a portion of said upper surface to a depth, thereby forming an opening having a bottom surface, a mouth, and side walls;

placing said integrated circuit in a sputtering chamber;

in said sputtering chamber, by connecting a metal target to said power supply, set to high voltage, sputter depositing a seed layer of metal to coat the integrated circuit upper surface, the bottom surface, and the side walls of the opening;

then, in said sputtering chamber, by connecting said integrated circuit to said power supply set to low power and voltage, sputter etching the seed layer, to reduce its thickness by an amount, thereby preferentially removing any overhang present at the mouth of the opening; and

~~depositing~~ forming an additional metal~~, whereby~~ in said opening ~~becomes completely filled with void free metal~~.

13. (Currently Amended) The process described in claim 12 wherein said power is between about ~~1 and~~ 1KW and 50KW.

14-27. (Cancelled).